BB-762: DESIGN AND IMPLEMENTATION OF 762 PROCESSOR MULTIPROCESSOR AND OCP-IP BENCHMARKING

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Abstract

Design productivity is one the most important challenge facing future generation multiprocessor system on chip (MPSOC). The design productivity concerns hardware as well as software issues however sofwtare design productivity is more challenging especially for parallel software.

1. Introduction

The ITRS Semiconductor roadmap projects that hundred of processors will be needed for future generation MPSOC designs [1]. Multi-FPGA platform emulation is the only way to implement these large scale multiprocessors and emulate application requiring billion cycles. We have implemented a multiprocessor of 762 cores connected by Network on Chip (NoC) on a commercial Multi-FPGA platform, Zebu-XXL of Eve [8] with 56 Xilinx virtex-4 LX200 [5].

2.BB-762 Multiprocessor Architecture

We reuse our basic small scale multiprocessor (SSM) [3], and extend it to the 56 FPGA to build the 762-core multiprocessor. The architecture of the small scale multiprocessor in figure 2 is based on a mesh-based network on chip connecting 12 processors organized as with 3 processors and 2 SRAM on chip memories per switch. The network on chip topology is mesh for a better multi-FPGA implementation. The selected embedded processor is the MicroBlaze processor soft IP [5] which is flexible, and gives the user control of a number of execution units like: hardware divider (HWD), and floating point unit (FPU). Other user defined coprocessor can be connected to MicroBlaze and greatly improve the system's performance. This SSM IP is a soft multiprocessor IP which is fully configurable in the embedded processor, on chip memory and network on chip parameters. The 12 processors are organized as 4 clusters of 3 processors (M_i) and 2 memories (S_i). Clusters are connected through a 2x2 mesh based network on chip. The network on chip is based on wormhole routing.

The BB-762 multiprocessor architecture is based on a large scale emulator composed of 64 FPGA.

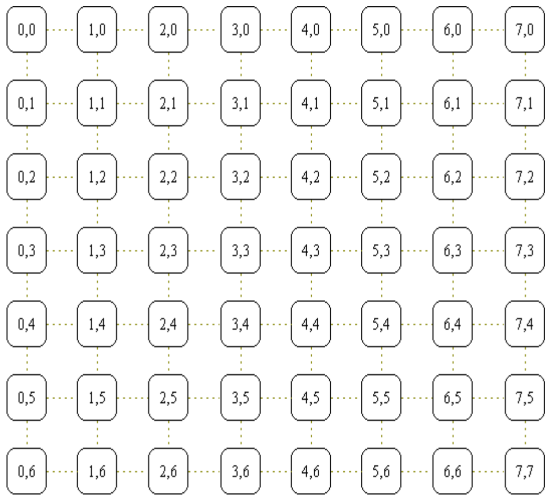

Figure 1: BB-762 7x8 FPGA emulator

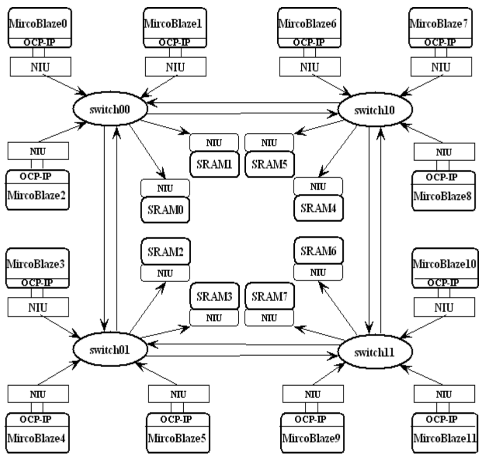

Figure 2: SSM IP

3. BB-762 Hardware Implementation

The BB-762 multiprocessor have been desigend based on the following IPs.

TABLE I - IPS FOR MULTIPROCESSOR DESIGN

IP component	Description	Source	Version
processor	Soft core IP	Microblaze Soft core IP Xilinx	5.00 b
memory	Soft core IP	Xilinx Coregen 96KB	v.2.4.
Network on chip switch	Soft core IP	VHDL Arteris Danube library	1.10
Interchip	Soft core IP	VHDL Arteris Danube library	1.10

Our emulation platform is the Eve Zebu-XXL Platform. The ZeBu-XXL platform is based on 64 Xilinx Virtex-4 LX200 chips.

Figure 3 : Eve Zebu-XXL Platform.

The 64 FPGA based system can emulate the equivalent of up to 100 million ASIC gates in a single card.

4. Performance Evaluation

The OCP-IP NoC micro-benchmark has been emulated on this multiprocessor, and performances like latency and throughput have been measured using hardware monitoring components. Probes are added to the input and output ports of each MicroBlaze, and each packet is measured and the performances are calculated and collected by the component Static-collector. Results in figure 4 shows that the latency of each processor on different FPGA is diverse.

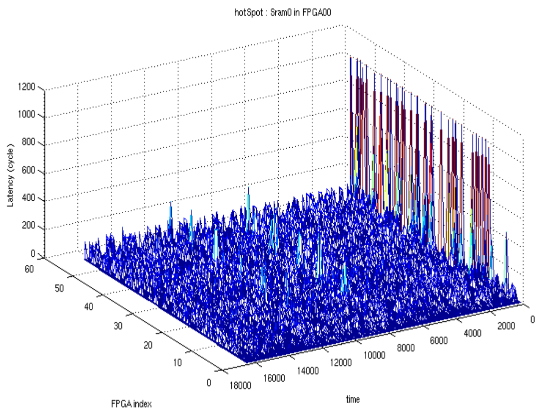

Figure 4 : OCP-IP Benchmarking

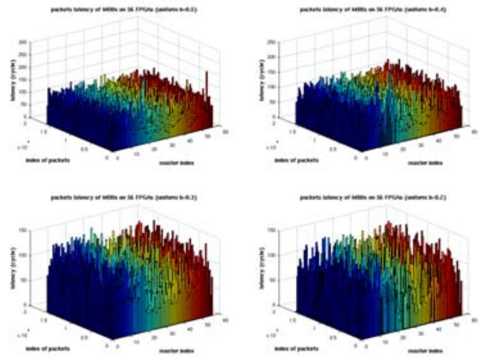

Figure 5 : OCP-IP Benchmarking

Future work include porting several benchmarks [9-11] and conducts large scale design space exploration.

4. Conclusion

Embedded multiprocessor software design productivity is a major challenge.

We propose BB-762 as an university community platform to conduct federated research on multiprocessor design, performnce evaluation studies and measurements.

We are currently porting several parallel applications from various domains cryptography, software defined radio) and explore tasks placement effects. Network on chip monitoring provides real time feedback to the parallel programmers.

To the best of our knowledge this is the first OCP-IP based large scale multiprocessor design and evaluation of OCP microbenchmarks.

5. References

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