

MPFPGA-LIB: A FAMILY OF SOFT MULTIPROCESSOR WITH NOC FROM 12 TO 48 PROCESSORS

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Abstract

Design productivity is one the most important challenge facing future generation multiprocessor system on chip (MPSOC). The design productivity concerns hardware as well as software issues however software design productivity is more challenging especially for parallel software. The MPFPGA-LIB project aims at providing a family of soft IP multiprocessors executable on FPGA to help software developpers easily map their application on various platforms. The MPFPGA-LIB contains a 12, 24 and 48 processors multiprocessor with network on chip based on mesh topology. The library has been designed and validated through multi-FPGA emulation on a set of linear algebra applications.

1. Introduction

ITRS Semiconductor roadmap [1] projects that hundred of processors will be needed for future generation MPSOC designs. Among the various challenges of MPSOC [2] software design productivity is paramount. Embedded multiprocessor software developpers have to map their application under resources constraints and may not reach the target performance requirements on a given architecture. They have to jointly explore parallel software implementations and embedded multiprocessor architectures. The MPFPGA-LIB provides 3 architectures on which embedded software developpers can map their applications and find a tradeoff between parallel software performance and architecture resources.

2. MPFPGA-LIB Multiprocessor Architecture

The MPFPGA-LIB architecture is based on the Small Scale

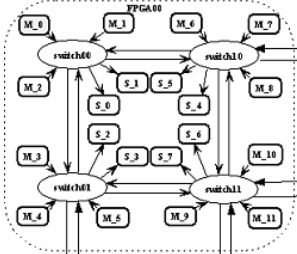


Figure 1: MPFPGA-LIB: 12-processors multiprocessor version

Multiprocessor (SSM IP) [8]. This SSM IP is a soft multiprocessor IP which is fully configurable in the embedded processor, on chip memory and network on chip parameters. The MPFPGA-LIB multiprocessor library is

organized as a family of mesh based distributed memory multiprocessor architecture with 12, 24 and 48 processors based on the SSM IP. Figure 1 describes the 12 processor version which can be easily extended. The 12 processors are organized as 4 clusters of 3 processors (M_i) and 2 memories (S_i). Clusters are connected through a 2x2 mesh based network on chip. The network on chip is based on wormhole routing.

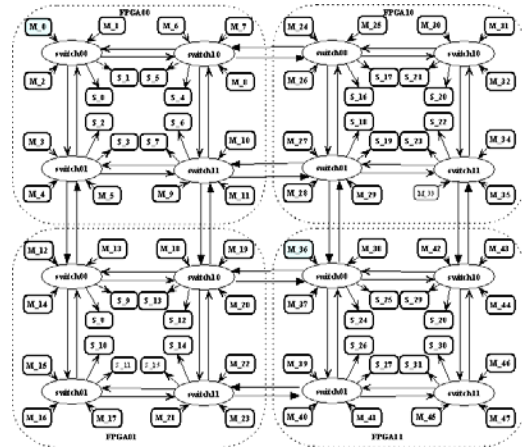


Figure 2: MPFPGA-LIB 48-processors multiprocessor version

The 48 processors version is described Figure 2 and represents a natural extension to the 12 processors version the SSM IP.

3. MPFPGA-LIB Implementation

Due to its large size and prohibitive simulation time parallel software design space exploration can be more efficiently tackled through emulation. We have implemented the MPFPGA-LIB based on the following IPs.

TABLE I - IPS FOR MULTIPROCESSOR DESIGN

IP component	Description	Source	Version
processor	Soft core IP	Microblaze Soft core IP Xilinx [10]	5.00 b
memory	Soft core IP	Xilinx Coregen [10] 96KB	v.2.4.
Network on chip switch	Soft core IP	VHDL Arteris [9] Danube library	1.10
Interchip	Soft core IP	VHDL Arteris [9] Danube library	1.10

Our emulation platform is the Eve Zebu-UF4 Platform. ZeBu-UF4 platform [13] is based on 4 Xilinx Virtex-4 LX200, built as an extended PCI card via a motherboard-daughter card approach.



Figure 3: Eve Zebu-UF4 Platform.

The 4 FPGA based system can emulate the equivalent of up to 6 million ASIC gates in a single card. ZeBu-UF also includes on-board memory capacity based on 64 MBytes of SSRAM and 512 MBytes of DRAM memory chips via an additional memory board, which plugs into the PCI motherboard.

TABLE II
EVE ZEBU-UF4 PLATFORM DETAILS

Modules	Descriptions
FPGA	4 Virtex-4 LX200
DRAM	512 MBytes
SSRAM	64 MBytes
ICE	Smart and Direct

4. Performance Evaluation

Applications of dot product and matrix multiplication are tested on this platform. Each MicroBlaze calculates a dot product or matrix multiplication of dimension 800*800.

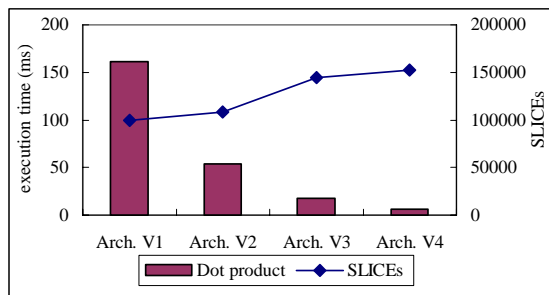


Figure 4: Execution time of Dot Product.

All the variables are floating point numbers to show the impact of FPU units. A global synchronization is used to make sure all the calculations are finished. The floating point unit (FPU) can greatly improve the performance of MicroBlaze and the pipelines of NoC can improve the system timing. The system performance can be improved by one magnitude.

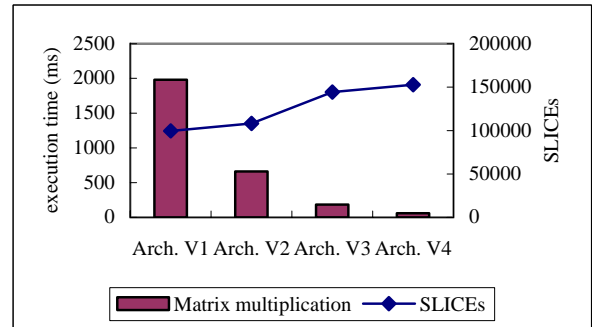


Figure 5: Execution time of Matrix Multiplication.

Future work includes porting several benchmarks [3-7] and analyzes parallelisms at various levels loop level [11], thread level and multiprogramming [12].

4. Conclusion

Embedded multiprocessor software design productivity is a major challenge. We propose MPFPGA-LIB a library of fully parametrizable multiprocessor soft IP which have been validated and executed through multi-FPGA emulation. We are currently porting several parallel applications from various domains cryptography, software defined radio) and explore tasks placement effects. Network on chip monitoring provides real time feedback to the parallel programmers. To the best of our knowledge this is the first library of soft multiprocessors IP.

5. References

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